REMARKS

The Office Action dated March 8, 2007 has been received and considered. In this response, claims 1 and 16 have been amended. Support for the amendments may be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claims 9-15

The Applicant notes with appreciation the indication at page 7 of the Office Action that claims 9-15 are allowed.

Obviousness Rejection of Claims 1-8 and 16-18

At page 2 of the Office Action, claims 1-8 and 16-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baird (U.S. Patent No. 6,204,787 B1) in view of Ferguson, Jr. et al. (U.S. Patent No. 6,040,793) and further in view of Van Herzeele (U.S. Patent No. 6,400,295 B1). This rejection is hereby respectfully traversed.

Claim 1 recites "a second set of switches coupled between the pair of capacitors and the integrator input, the second set of switches configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component." These elements are not disclosed by the cited references. As asserted by the Office Action at page 3, Baird "fails to specifically disclose the second set of switches." Accordingly, the Office Action relies on Ferguson as disclosing the second set of switches.

According to the Office Action at page 3, Ferguson discloses the second set of switches at FIG 2, items 51 and 56, and at column 6, lines 14-17, 29-32 and column 8, lines 6-9. Accordingly, the Office Action implicitly identifies the pair of capacitors as recited in claim 1 as capacitors C1 and C2 and the second set of switches as recited in claim 1 as switches S3, S4, S7, S8. *Ferguson*, FIG. 2. Further, the Office Action implicitly identifies nodes 93 and 95 of Ferguson as the integrator inputs recited in claim 1. However, claim 1 presently recites that the second set of switches are coupled between the pair capacitors and the input of the integrator, and that they are configured to transfer a first charge proportional to a reference voltage and a second charge to the integrator input, the second charge proportional to the DC offset

component. However, as illustrated in FIG. 2 of Ferguson, none of the switches S3, S4, S7 and S8 are configured to transfer a first charge proportional to a reference voltage and a second charge proportional to a DC offset to the integrator input. *Id*. Instead, the switches S3, S4, S7 and S8 are configured to deliver an input voltage (Vin) to the integrator input. *Id*. Accordingly, Ferguson does not disclose or suggest a second set of switches coupled between the pair of capacitors and the integrator input, the second set of switches configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component as recited in claim 1. Further, Baird and Van Herzeele do not remedy the deficiencies of Ferguson. Accordingly, the cited references fail to disclose or suggest each and every element of claim 1.

Claims 2-8 depend from claim 1. Accordingly, the cited references fail to disclose or suggest each and every element of these claims, at least by virtue of their dependence on claim 1. In addition, claims 2-8 recite additional novel elements.

With respect to claim 16, the claim recites "during a second phase, transferring a sum charge via the pair of capacitors to inputs of a first integrator in a series of integrators in a sigma delta converter, the sum charge including the reference charge and a DC offset correction charge." The Office Action states at page 6 that "the elements in system claim 1 would have necessitated the steps in method claim 16" but does not identify which of the cited references discloses transferring a sum charge via a pair of capacitors to inputs of a first integrator in a series of integrators in a sigma delta converter, the sum charge including a reference charge and a DC offset correction charge." As indicated by the Office Action at page 3, neither Baird nor Ferguson discloses transferring a second charge proportional to a DC offset component. According to the Office Action at pages 3-4, these elements are disclosed by Van Herzeele, at FIG. 2, SC 5, FIGs. 3 and 4, column 7, lines 57-67, and column 8, lines 1-24. The cited portions of Van Herzeele show a configuration of switches to transfer a charge based on a DC offset to the input of an integrator via a pair of capacitors, C5P and C5N. *Van Herzeele*, FIG. 2. Van Herzeele specifically discloses that a charge based on a reference voltage (Pref and Nref) are provided **via a different pair of capacitors**, C3P and C3N. Thus, Van Herzeele discloses transferring a charge based on a reference voltage to an integrator input using one set of capacitors and transferring a charge based on a DC offset via a different set of capacitors. Van

Herzeele does not disclose or suggest transferring **a sum charge via a pair of capacitors** to inputs of a first integrator in a series of integrators in a sigma delta converter, the sum charge including the reference charge and a DC offset correction charge, as recited in claim 16. Accordingly, the cited references fail to disclose or suggest each and every element of claim 16.

Claims 17 and 18 depend from claim 16. Accordingly, the cited references fail to disclose or suggest each and every element of these claims, at least by virtue of their dependence on claim 16. In addition, claims 17 and 18 recite additional novel elements.

In addition, there is no motivation to combine the cited references. "If [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *MPEP* § 2143.01. In this case, each of the cited references disclose switched capacitor circuits connected to an integrator. *Ferguson*, FIG. 2, *Van Herzeele*, FIG. 2, *Baird*, FIG. 7A. However, the switches in the switched capacitor circuit of each cited reference are controlled by very different signals, with very different time relationships. *See, e.g., Baird*, FIG. 8 and *Ferguson*, col. 6, line 57 – col. 7, line 26. Because of these different time relationships, a combination of the circuits disclose in each reference would not be operable for its intended purpose. For example, if the signals used to control the switches in the Ferguson circuit were used to control the switches of the Baird circuit, the Baird circuit would be rendered inoperable for its intended purpose. Accordingly, one skilled in the art would not be motivated to combine the cited references, and that combination cannot be used as a basis for an obviousness rejection.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 1-8 and 16-18 is improper. Withdrawal of this rejection and reconsideration of the claims is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicant believes no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-3797.

Respectfully submitted,

/Adam D. Sheehan/ May 30, 2007
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